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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/709,096	04/13/2004	Kei MURAYAMA	040169	3095

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/25/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,096	MURAYAMA ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 8-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 8-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04/14/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-5 and 8-10 in the reply filed on November 8, 2005 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (US 6326561), hereinafter Watanabe.

Regarding claim 1, Fig. 10 of Watanabe shows a wing substrate [24, 22] in which a bump of an electronic part is bonded to a connection pad of the wiring substrate, which has a structure in which a wiring pattern [4 in Fig. 1] including the connection pad is provided on an insulating film [2], by a flip-chip packaging, wherein a via hole into which a via post [3; via stud] acting as a strut to support the connection pad upon the flip-chip packaging is filled is arranged in the insulating film under the connection pad.

Note that "by an ultrasonic flip-chip packaging" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 8, Fig. 10 of Watanabe shows that the insulating film on the wiring substrate is made of resin (col. 9, lines 41-44).

Regarding claim 9, Fig. 10 of Watanabe shows that the electronic parts whose bump is bonded to the connection pad of the wiring substrate.

Note that "by the ultrasonic flip-chip packaging" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe.

Regarding claim 2, Fig. 10 of Watanabe shows a wing substrate [24, 22] in which a bump of an electronic part is bonded to a connection pad of the wiring substrate, which has a structure in which a wiring pattern [4 in Fig. 1] including the connection pad is provided on an insulating film [2], by a flip-chip packaging, wherein a via hole into which

a via post [3; via stud] acting as a strut to support the connection pad upon the flip-chip packaging is filled is arranged in the insulating film under the connection pad.

Fig. 10 of Watanabe fails to show that a via hole is filled is arranged "in a predetermined portion of the insulating film under the wiring pattern connected to the connection pad within 200 um from the connection pad." However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have a via hole arranged in a predetermined portion of the insulating film under the wiring pattern connected to the connection pad within 200 um from the connection pad for compact package, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller,* 105 USPQ 233.

In addition, note that "by an ultrasonic flip-chip packaging" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Umematsu et al. (US 6399897), hereinafter Umematsu.

Regarding claim 3, Fig. 10 of Watanabe shows most aspect of the instant invention except "the via hole is a dummy via hole and a normal via hole is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad." Fig. 5B of Umematsu shows a semiconductor package with a wiring substrate [49] wherein the via

hole is a dummy via hole [58a] and a normal via hole[58] is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad [60].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Umematsu into the device of Watanabe in order to have the via hole to be a dummy via hole and a normal via hole arranged separately under a predetermined portion of the wiring pattern connected to the connection pad to alleviate a cracking with a dummy via and to have a signal connection with a normal via.

Regarding claim 5, the combined teachings of Watanabe and Umematsu show most aspect of the instant invention except "the normal via hole is arranged in a position that is away from the connection pad in excess of 200 um." However, it would have been obvious to one of ordinary skill in the art at the time of the invention made to have a normal via hole arranged in a position that is away from the connection pad in excess of 200 um for compact package, since it would have been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only in routine skill in the art. *In re Aller,* 105 USPQ 233.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Ohuchi (US 6590287).

Regarding claim 10, Fig. 10 of Watanabe shows most aspect of the instant invention except "the bump of the electronic parts is made of gold, and at least a surface layer portion of the connection pad of the wiring substrate is made of gold."

Fig. 5 of Ohuchi shows a semiconductor package wherein the bump [5] of the electronic parts is made of gold, and at least a surface layer portion of the connection pad [7] of the wiring substrate [1] is made of gold (col. 5, lines 41-45).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Ohuchi into the device of Watanabe in order to have the bump of the electronic parts made of gold, and at least a surface layer portion of the connection pad of the wiring substrate made of gold for easier soldering.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Umematsu and Minagawa et al. (JP-2002009444), hereinafter Minagawa.

Regarding claim 4, Fig. 10 of Watanabe shows most aspect of the instant invention except "a plurality of via holes associated with said plurality of connection pads are arranged in a state that a dummy via hole and normal via holes are arranged mixedly, and a normal via hole is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad, in the wiring pattern in which the dummy via hole is arranged under the connection pad or the wiring pattern."

Fig. 5B of Umematsu shows a semiconductor package with a wiring substrate [49] wherein the via hole is a dummy via hole [58a] and a normal via hole[58] is arranged separately under a predetermined portion of the wiring pattern connected to the connection pad [60].

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Umematsu into the device of Watanabe in order to have

the via hole to be a dummy via hole and a normal via hole arranged separately under a predetermined portion of the wiring pattern connected to the connection pad to alleviate a cracking with a dummy via and to have a signal connection with a normal via.

The combined teachings of Watanabe and Umematsu fail to show that "a plurality of via holes associated with said plurality of connection pads are arranged in a state that a dummy via hole and normal via holes are arranged mixedly." Fig. 1 of Minagawa shows a wiring substrate wherein a plurality of via holes [4, 7] associated with said plurality of connection pads are arranged in a state that a dummy via hole [7] and normal via holes [4] are arranged mixedly.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Minagawa into the device of Watanabe and Umematsu in order to have a dummy via hole and normal via holes arranged mixedly to withstand the pressure from the pad with a dummy via while conducting a signal with a normal via from the same pad.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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